REMARKS

Claims 1, 2, and 4-20 are pending and were rejected. Claim 3 has been canceled.

1. Rejections Under 35 U.S.C. § 103(a)

In the Office Action mailed February 7, 2007, the Examiner rejected claims 1-7 and 13-14 under 35 U.S.C. § 103(a) as being unpatentable over O'Connell et al. (U.S. 6,006,340) in view of Holm et al. (U.S. 6,687,225). The Examiner asserts that O'Connell discloses all elements of a bridge circuit for use in retiming a semiconductor integrated circuit recited in claim 1, except that O'Connell does not disclose that the storage locations are not read until a predetermined time delay. The Examiner states Holm discloses storage locations being read after a predetermined time delay. Applicant disagrees.

O'Connell and Holm do not teach or suggest that the storage locations are not read until a predetermined time delay. (See this feature in claim 1, last paragraph of the present invention.) Holm discloses starting to extract data from the FIFO only after a set amount of data is stored in the FIFO (Column 2, lines 4-7). The amount time necessary to fill the FIFO with a set amount of data is variable and is dependant upon the rate of data being sent to the FIFO in a particular situation. This rate can change depending on the data through put. Holm discloses reading from the FIFO after the FIFO is completely filled with data to avoid problems that may corrupt the transmission (Column 2, lines 9-16). Waiting until the FIFO is full requires delaying before beginning to transmit data from the FIFO. It is clear that in Holm, the threshold necessary to begin transferring data from the FIFO is not time dependent or based on some time delay.

Holm also discloses another type of counter that transmits data from the FIFO after a certain amount of time has passed (Column 2, lines 50-51). This is quite different from the present invention. In Holm, determining whether a certain amount of time has passed relates directly to the above mentioned threshold of a set amount of data. In Holm, difficulties occur when the amount of data held in the FIFO is not large enough to trigger the threshold amount (Column 2, lines 33-38). In order to ensure smaller groups of data are not left in the FIFO,

Holms discloses a controller that begins transmitting the data held in the FIFO if the FIFO was not empty and more than a selected amount of time had passed. Holms does not disclose a predetermined time delay whose purpose is to delay the output of the data in the FIFO in order to allow the data to accumulate in the FIFO and be read back to back. Holm may often transmit before this set time has passed if sufficient data has been stored. Holm requires the transfer to start if too much time has passed; for the present invention, transfer is prevented until after a certain time has passed; these are the exact opposite. Holm teaches away from the invention.

For the foregoing reasons, claim 1 is nonobvious in view of the cited prior art. Claims 2, 4-7, and 12-14 depend from claim 1, and thus, are not taught or suggested by O'Connell and Holm.

Claims 8-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over O'Connell, in view of Holm, and in further view of Sadowski (U.S. 2005/007165).

O'Connell, Holm, and Sadowski do not teach or suggest the invention recited in claim 8, which is dependent upon claim 1. First, Sadowski does not teach or suggest any of the features of claim 1 that are missing from O'Connell and Holm. Second, Sadowski does not teach or suggest a retiming circuit adapted to provide a plurality of possible degrees of retiming, including a mode signal input for receiving a mode signal indicating the currently required degree of retiming, the retiming circuit being responsive to the mode signal to provide the required degree of retiming.

Sadowski discloses a system for determining the processing speed of an integrated circuit, where a multiplexer receives a select delay signal indicating which one of the delays is to be chosen as an output signal [0018]. Sadowski selects a delay signal from a plurality of clock-adjusting circuits 124, 126, 128, and 130 which are similar to the delay circuit 120 [0017]. The clock adjusting circuits generate possible degrees of delay, but do not teach possible degrees of retiming a signal into a specific clock domain. The clock adjusting circuits of Sadowski are not clocked and therefore can not retime a signal to a clock source.

For the foregoing reasons, claim 8 and claims 9-11, which depend from claim 8, are nonobvious view of the cited prior art.

Claims 15-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over O'Connell, in view of Holm, and in further view of Sadowski. The Examiner asserts that O'Connell discloses all elements of a bridge circuit for use in retiming a semiconductor integrated circuit recited in claim 15, except that O'Connell does not disclose a selector connected to receive inputs from each of the retiming buffers and a storage buffer control circuit that is adapted to control the selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparators. The Examiner asserts Sadowski discloses a selector connected to receive inputs from each of the retiming buffers and a storage buffer control circuit adapted to control the selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparators.

O'Connell, Holm, and Sadowski do not teach or suggest the invention recited in independent claim 15. As described above, Sadowski discloses a system for determining the processing speed of an integrated circuit, where a multiplexer receives a select delay signal indicating which one of the delays is to be chosen as an output signal [0018]. A multiplexer selects the amount of latency or delay added into the signal path. The clock-adjusting circuits 124, 126, 128, and 130, which are similar to the delay circuit 120, are not retiming buffers. Even though the delay elements of Sadowski introduce a degree of delay into the circuit, the clock adjusting circuits are not clocked and therefore do not retime an input signal to a clock source.

Sadowski also discloses a sequencer capable of selecting different clock speed adjusting circuits to determine the processing speed of the integrated circuit [0024]. Although the sequencer controls selection of the clock adjusting circuits, the sequencer does not receive inputs from each of the retiming buffers. The sequencer of Sadowski does not teach or suggest a storage buffer control circuit adapted to control the selectors such that zero or more retiming buffers are selectively in the path from the read or write pointer registers to the comparators

For the foregoing reasons, claim 15 and claims 16-20, which depend from claim 15, are nonobvious view of the cited prior art. Further, in light of the remarks, the applicant respectfully submits that all rejections have been traversed and that pending claims 1-20 are allowable.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/David V. Carlson/

David V. Carlson
Registration No. 31,153

DVC:lcs

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

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